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Design Technique using Extra Fast-cornered Transistors to Reduce Random Telegraph Signal Noise in a CMOS Image Sensor

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ABSTRACT

This paper proposes a simple but effective design technique to reduce the random telegraph signal (RTS) noise in a CMOS image sensor (CIS). Through the analysis of the characteristics of the RTS noise, we conclude that the RTS noise can be effectively reduced by using extra fast-cornered transistors in the input stage of a comparators which are used in the CIS with a column-wise correlated-double sampling (CDS)/single-slope analog-to-digital converter (ADC) circuit array. Since there is no way to verify the validity of the proposed design technique in SPICE simulation due to lack of the RTS noise model in the transistor model parameter, we have prepared the fabricated CIS chip which contains an array of column-wise ADCs with analog/digital CDS function to confirm the proposed design technique and are testing the fabricated CIS chip to verify the validity of the proposed design technique.

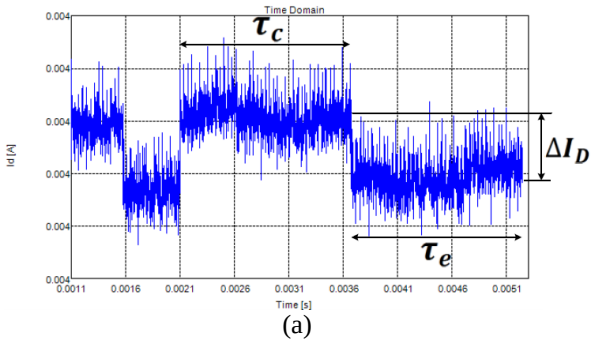
Keywords: random telegraph signal noise; RTS noise; CMOS image sensor, column-wise CDS/ADC; single-slope ADC; correlated double sampling.

INTRODUCTION

CMOS image sensors (CIS) are used extensively in consumer electronics due to its attractions such as low power consumption, applicability for integration of photodetecting devices like a photodiode with readout and signal processing circuits, free accessibility to a certain address, and so on. As the requirement for high-end CMOS image sensors are growing, a correlated-double sampling (CDS) technique is widely used to reduce temporal and fixed noises such as reset, 1/*f*, and DC offset. However, it cannot fully remove the random telegraph signal (RTS) noise which becomes very important these days as process become scaled down aggressively.

Although there have been much progress by many researches such as using a switched-biasing technique [1], increasing size of target transistors [2], applying a trench corner rounding (TCR) process [3], and using buried-channel transistors [4] to reduce the RTS noise nowadays, it is necessary for the RTS noise to be reduced more for improved image quality.

In this paper, we propose a simple but effective design technique which uses extra fast-cornered transistors instead of normal ones in the most noise-contributing transistors to reduce the RTS noise and analyze how it works. The proposed method can be applied additionally to the existing solutions and improve the sensor's performance more with a little extra effort.



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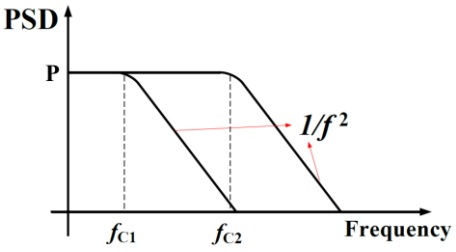


(b)

Fig. 1: RTS noise affecting drain current in the time domain and the frequency domain.
(a) Drain current fluctuation in time domain
(b) Spectral response of the RTS noise

The rest of the paper is organized as follows. Next, the characteristics of the RTS noise is described. Section 3 proposes the design technique to reduce the RTS noise. Section 4 is devoted to the implementation of a CIS and limitations on verifying the proposed method through the simulation. Finally, conclusions are provided in Section 5.

Characteristics of The Rts Noise:

As the CMOS technology has developed continuously, the transistors become very small. As a result, internal noise disturbing drain current is dominated by the capture/emission phenomenon of a single active defect located near the Si/SiO_2 interface and in the oxide layer.

Capture/emission of an electron leads to change the threshold voltage of the transistor and make the drain current switching between two states as shown in Fig. 1 and we call this a RTS noise. In Fig. 1, its frequency spectrum is also shown which has a Lorentzian spectrum characterized by a constant plateau, P and a roll-off which has a slope of $1/f^2$ and a cut-off frequency of f_c. There are several important factors featuring the RTS noise such as τ_c, τ_e, f_c and ΔI_D where τ_c and τ_e means average capture/emission time respectively, f_c is the cut-off frequency, and ΔI_D is the amount of current fluctuation. Then the power spectrum density (PSD) of it can be expressed as:

$$S_I(f) = \frac{P}{1 + \left(\frac{f}{f_c}\right)^2} \quad (1)$$

$$P = \left(\frac{4}{\tau_c + \tau_e}\right)\left(\frac{\eta g_m q}{WLC_{ox}}\right)^2 \quad (2)$$

$$f_c = \frac{1}{2\pi}\left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right) \quad (3)$$

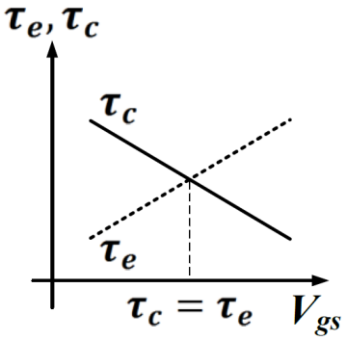
where g_m means a transconductance, ŋ is a fit parameter, and W and L are the width and the length of the transistor respectively.

The capture/emission time constants can be described by the Shockley-Read-Hall theory [1]. Considering an n-channel MOSFET, the electron density increases as V_{gs} increases and as a consequence, τ_c decreases. τ_e features an opposite dependence on V_{gs} due to the gate-field dependence of the trap energy E_T and of the tunnelling probability affecting the trap capture cross section. As mentioned, when the τ_c decreases and τ_e increases when the gate-source voltage, V_{gs} increases and therefore, PSD is also changed with V_{gs}.

Proposed Design Technique To Reduce Rts Noise:

To reduce the RTS noise, it is necessary to decrease Lorentzian plateau, P or move the cut-off frequency f_c far from the maximum point where both time constants are the same. Increasing the size of the transistor is a straightforward way to achieve it. However, net die will decrease with this and also there can be a limitation in designing the CIS that every circuit should be included in a narrow pixel pitch. g_m is a design parameter which can decide the amplifier's gain and so on. Therefore, it will be determined by the design specifications.

As mentioned above, the time-constants are changed by V_{gs}. That is, if we change the V_{gs} while maintaining g_m, both P and f_c will be also changed. If the operating point of the target transistor (V_{gs}) is in the region ① of Fig. 2(b), decreasing V_{gs} makes the ratio between τ_e and τ_c decrease and thus, f_c will also decrease [1]. If the operating point is in the region ②, increasing V_{gs} will help to reduce f_c. If the plateau P is constant as shown in Fig 2(c), the noise power will be reduced with lower f_c at a fixed operating frequency.



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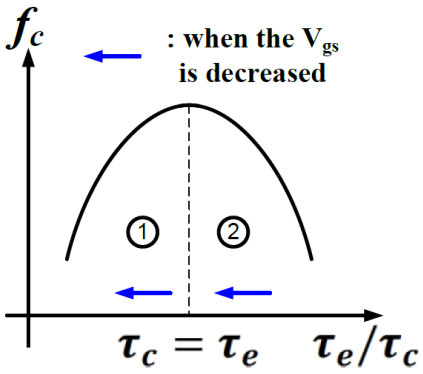

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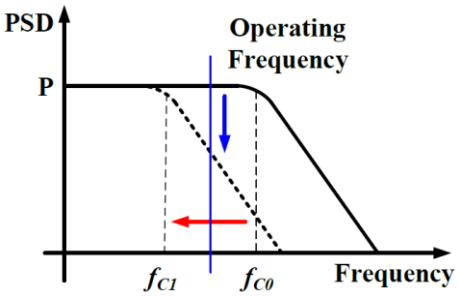


(c)

Fig. 2: RTS noise characteristics according to the V_{gs}.
(a) τ_c and τ_e functions of V_{gs}
(b) f_c functions of τ_c and τ_e and V_{gs}
(c) Effect of decreased f_c in frequency domain

Of course, the time constants, τ_e and τ_c are dependent on the characteristics of the semiconductor fabrication process absolutely and their slopes can be different according to circumstances. However, the sum of those two constants does not change so much, because they have contrary characteristics to V_{gs}. On the other hand, the actual noise power will be reduced much as f_c decreased, because the PSD has roll-off slope of $1/f^2$.

Both decreasing and increasing V_{gs} can be achieved by using fast- or slow-cornered transistors rather than normal ones, because they have smaller or larger threshold voltage, V_{th}. Between two methods, we will select the method to decrease V_{gs}, because it can retain high dynamic range (DR) performance and high speed performance of the analog circuits. If there is a constant current source, I_{DQ} connected to a certain transistor, then using a fast-cornered transistor leads the V_{gs} to decrease as

$$V_{gs} = \sqrt{\frac{2L}{kW} I_{DQ}} + V_{th} \quad (4)$$

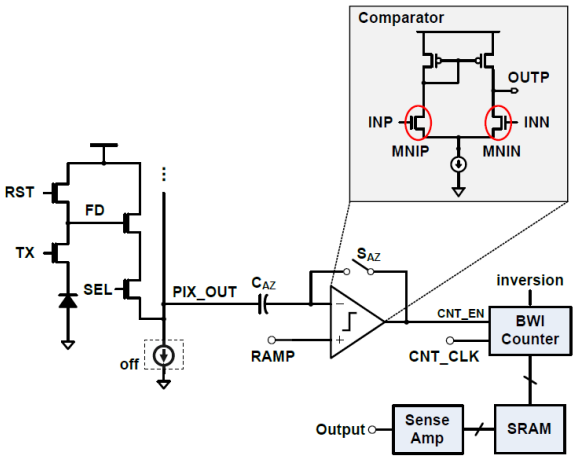
because V_{th} decreases and thus the noise power will be reduced when the V_{gs} is in the region ①. However, its transconductance, g_m will be the same because the overdrive voltage V_{gs} - V_{th} will be constant [6]. As the transistor is more far from normal corner, the more RTS noise power can be reduced due to smaller V_{gs}.

Implementation of A Cis And Limitations on Verifying The Proposed Method:

The fabricated CIS chip has an array of the

common column readout circuits which perform CDS function and data converting simultaneously as shown in Fig. 3. This readout circuit combines the analog and digital CDS functions which reduce the reset conversion time of the digital CDS by cancelling the analog offset of pixel and comparator through the analog CDS and the digital CDS eliminates vertical FPN caused by the imperfect analog CDS and the decision delay variations.

The digital CDS is implemented using bit-wise inversion (BWI) column level counter. Fig. 3(b) shows the readout timing chart of the circuit in Fig. 3(a). The readout sequence is as follows:



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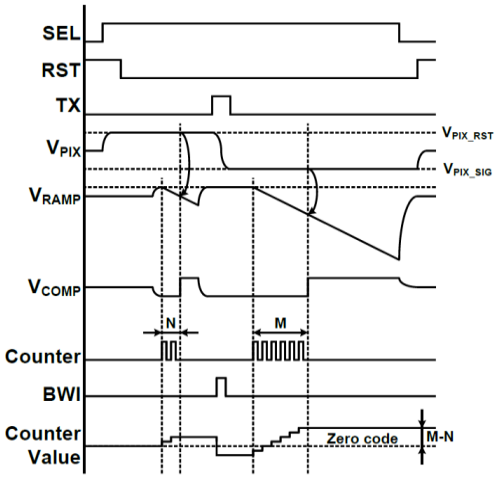

(b)

Fig. 3: RTS noise affecting drain current in the time domain and the frequency domain.
(a) Pixel and CDS circuits
(b) Operation timing diagram

1) A row of pixels are selected and reset.

2) The pixel output settles to reset level, and the input and the output of the comparator is connected through switch S_{AZ} to perform the analog CDS.

3) An offset is applied to ramp signal to make the following reference level ADC ramp cover the variation caused by imperfect the analog CDS and decision delay.

4) The reference level ADC is performed to measure the residual analog offset and decision delay variation. The BWI counter counts up whenever CNT_EN is high during the reference level ADC period.

5) The pixel signal is transferred and pixel output signals goes down to the pixel signal level. During the transfer period, every bit of BWI counter is inverted to perform 1's complement operation. Then the BWI counter holds negative value of the reference level ADC result. The digital CDS is performed by counting up the following pixel signal ADC result from the negative value of reference level ADC result.

6) After the pixel signal ADC, the BWI counter value is transferred to column SRAM and pipelining the SRAM readout and the following row A/D conversion. It is noted that the noise sampled in the

auto-zero capacitor C_{AZ} is eliminated by the digital CDS.

In this way, this circuit extracts only digital code for light signal as (M-N). We have excluded the RTS noise from pixels by turning off the current source and therefore the noise in the image would be from the comparator only. When we use an n-type differential amplifier as a comparator as depicted in Fig 3, two input transistors MNIP and MNIN are the most noise contributing ones [6]. Therefore, the proposed design technique should be applied to these two transistors. Because the amplifier has input transistors of n-type MOSFET, we have to move them to extra-fast corner to reduce the V_{th} and V_{gs}.

To confirm the proposed design technique, it is necessary to simulate the CIS circuit in SPICE or test the fabricated CIS. However, one big drawback is that it is hard to verify the proposed design technique in SPICE simulation. There are only thermal and 1/f noise model in the SPICE library and it does not contain the RTS noise model. Therefore, the proposed method should be verified with a fabricated CIS chip and the test results will surely show that this method reject the RTS noise effectively. We are testing the fabricated CIS chip to verify the validity of the proposed design technique.

Conclusions:

We proposed a simple but effective way which uses extra fast-cornered transistors in the input stage of a comparator in the CDS circuit to reduce the RTS noise in a CIS. By using extra-fast transistors instead of normal ones of the comparator in a CIS readout circuit, the V_{gs} and the noise power can be reduce with decreased f_c. Although there is no way to confirm this method in simulation due to absence of RTS noise model in the SPICE model parameter, we can see its effectiveness with fabricated sensor. The biggest advantage of this method is that it can be applied additionally to the existing solutions without any performance degradation, size extension, or special design. Therefore, it is expected that it will help to suppress the noise in wide applications.

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References

1. Zanolla, N., D. Siprak, M. Tiebout, P. Baumgartner, E. Sangiorgi and C. Fiegna, 2010.'Reduction of RTS noise in small-area MOSFETs under switched bias conditions and forward substrate bias', IEEE Trans. Electron Devices, 57(5): 1119-1128.
2. Leyris, C., F. Martinez, A. Hoffman, M. Valenza and J.C. VIldeuil, 2007. 'N-MOSFET oxide trap characterization induced by nitridation process using RTS noise analysis', Microelectronics Reliability, 47(1): 41-45.
3. Wang, R., Y. Lee, Y.R. Lu, W. McMahon, S. Hu and A. Ghetti, 2009.'Shallow trench isolation edge effect on random telegraph signal noise and implications for flash memory', IEEE Trans. Electron Devices, 56: (9): 2107-2113.
4. Chen, Y., X. Wang, A.J. Mierop and J.P. Theuwissen, 2009.'A CMOS image sensor with in-pixel buried-channel source follower and optimized row selector', IEEE Trans. Electron Devices, 56(11): 2390-2397.
5. Lim, Y., K. Koh, K. Kim, H. Yang, J. Kim, Y. Jeong, S. Lee, H. Lee, S.H. Lim, Y. Han, J. Kim, J.C. Yun, S. Ham and Y.T. Lee, 2010. 'A 1.1e- temporal noise 1/3.2-inch 8Mpixel CMOS image sensor using pseudo-multiple sampling'. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pprs, San Francisco, CA, USA, pp: 396-397.
6. Razavi, B., 2001. 'Design of analog CMOS integrated circuits' (McGraw Hill,)