Advances in Natural and Applied Sciences, 7(1): 33-38, 2013
ISSN 1995-0772

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# ORIGINAL ARTICLE

## Low Voltage Schmitt Trigger In 0.18 µm CMOS Technology

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Faiz Bin Arith, Md Mamun, Mohammad Arif Sobhan Bhuiyan and Ahmad Ashrif A. Bakar: Low Voltage Schmitt Trigger In 0.18 µm CMOS Technology

**ABSTRACT**

Schmitt Trigger circuit is widely used in analogue and digital circuit to solve the noise problem. Hysteresis is a common drawback of the Schmitt Triggers which is determined by the device dimensions, process parameters and supply voltages. This study presents a Schmitt Trigger circuit which can operate at low voltage. The proposed circuit is designed based on Conventional Schmitt Trigger by manipulating the arrangement of transistors' width-length ratio. The design is carried out in 0.18 µm CMOS technology using Mentor Graphics. From the simulation results, it is found that the proposed design can operate as low as 0.8V. The circuit offers less propagation delay compared to the conventional circuit. It can be widely used in various low voltage analogue and digital applications.

***Key words:*** CMOS, Capacitance, Hysteresis Schmitt Trigger, Transistor

### Introduction

The Schmitt trigger, introduced by Otto Schmitt in 1930s (Schmitt, 1938), has been commonly used in the field of communication and signal processing techniques for improving on/off control, reducing the noise effects in triggering devices, analogue to digital conversion (Mohd-Yasin *et al*., 2004; Reaz *et al*., 2007; Marufuzzaman *et al*., 2010; Chavez, 1995; Akter *et al*., 2008) and a number of other emerging applications including frequency doublers, retinal focal-plane sensors, sub-threshold SRAM, image sensors, pulse width modulation circuits, wireless transponders, FPGA based system and sensors etc. (Dejhan *et al*., 2004; Reaz *et al*., 2006; Reaz and Wei 2004; Mogaki *et al*., 2007; Yuan, 2009; Reaz *et al*., 2003; Romli *et al*., 2012; Reaz *et al*., 2005; Singhanath *et al*., 2011). A common drawback of Schmitt triggers is the hysteresis determined by the device dimensions, process parameters and supply voltages(Kuang, and Chuang, 2001). As a result, the hysteresis varies with process conditions and a spread of the parameters has to be tolerated from chip to chip as well as from batch to batch.

Several approaches have been proposed to implement Schmitt trigger(Kader *et al*., 2012). A conventional Schmitt trigger is shown in Fig. 1. A detailed design was proposed by Filanovsky and Baltes (1994) where the switching thresholds are dependent on the ratio of NMOS and PMOS. However, the design exhibited racing phenomena when the transition started. A low voltage Schmitt trigger is proposed in this paper which can operate from 0.8V-1.5V at high capacitance with less propagation delay and stable hysteresis width by lowering the supply voltage (Kulkarni and Roy, 2012; Lotze and Manoli, 2012).

### Materials And Methods

The proposed design is a combination of two sub-circuit, P Sub-Circuit (which consists of P1, P2 and P3) and N sub-circuit (which consists of N1, N2 and N3) as in Fig. 2.

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*Adv. in Nat. Appl. Sci., 7(1): 33-38, 2013*

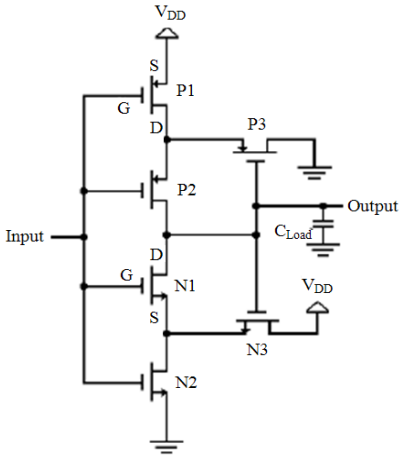


**Fig. 1:** The Conventional Schmitt Trigger

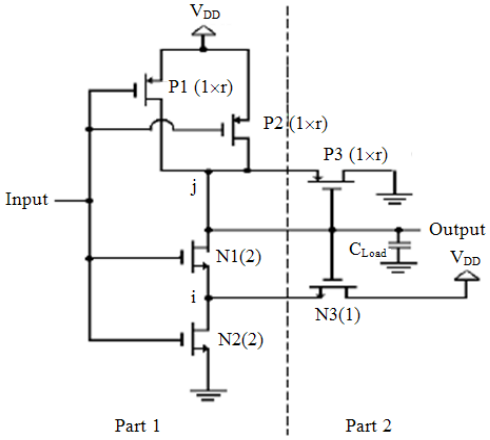


**Fig. 2:** The proposed Schmitt Trigger

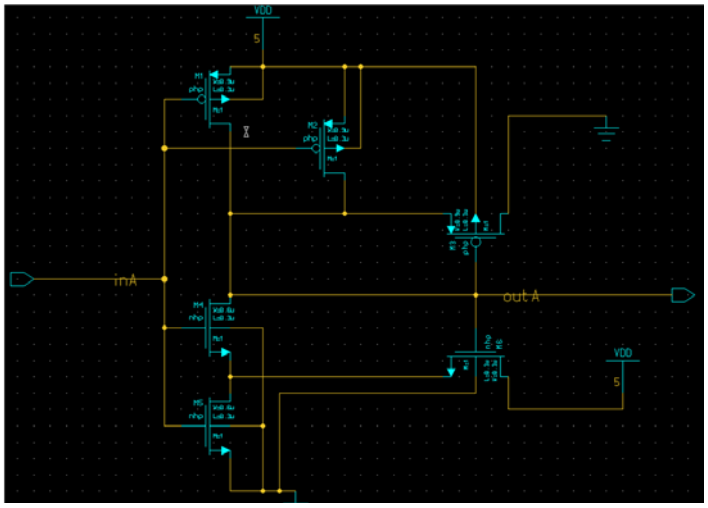


**Fig. 3:** Schematic diagram of the proposed Schmitt Trigger circuit

There is no direct connection between the source voltage and ground as P sub-circuit is connected to the path between the source voltage and output while the N sub-circuit is connected between the path of output and

ground. Therefore, there is no static power consumption as there is no direct path between source voltage and ground.

Part 1 of the proposed circuit forms a NAND gate and designed according to De Morgan`s Theorem. Two PMOS (P1 and P2) are formed by a parallel connection while two NMOS (N1 and N2) are formed by a series connection. By designing the PMOS in parallel, the resistance of the P sub-circuit will be reduced by halves. Thus, the propagation delay can be reduced as shown in Equation 1:

$$t_P = 0.69RC_L = \frac{t_{PHL} + t_{PLJH}}{2} \quad (1)$$

The PMOS delay is reduced because delay is more concentrated to PMOS due to high mobility of PMOS compared to NMOS. Part 2 of the proposed schmitt trigger consists of a PMOS, (P3) and a NMOS, (N3) where both the MOSFET is directly connected through the gate terminal of each. The P3 act as pull up while the N3 act as a pull down for the output at each case.

The sizes of the transistors are set by locating the minimum component path of each sub-circuit. Each of the transistors is sized according to their arrangement. The transistors in series are scaled by factor of 2 each while transistors in parallel are scaled by a factor of 1each. The PMOS and NMOS ratio is set according to Equation 2 with the effective length, Leff = 0.18 □m (for 0.18 technologies).

$$\left(\frac{W}{L_{eff}}\right)PMOS = r\left(\frac{W}{L_{eff}}\right)NMOS \quad (2)$$

The PMOS transistor is widen so that the resistance matches the pull down NMOS device. Typically, r = 3→3.5 (Sapawi *et al*., 2008). Therefore, the ratio is set to 3 to maximize the noise margin and to create a circuit with symmetrical Voltage-Transfer Characteristic (VTC). By increasing the width of PMOS, it moves the switching threshold voltage towards VDD, which makes the hysteresis width more rectangles as desired by a Schmitt trigger design.

When the input is low, only the P sub-circuit will be considered and causes the output to be high (equal to VDD). During this condition, both P1 and P2 are on, but P3 is off (because VSG<|Vtp| as P3's source voltage and gate voltage is equal). Therefore, the output voltage is pulled to VDD. When the input increases to VDD, N1 and N2 is turned on. Thus, the output voltage is pull down to ground. Mentor Graphic has been used to for designing the proposed Schmitt Trigger. The schmetic diagram is shown in Fig. 3.

## Results And Discussions

The Three designs are simulated using Mentor Graphic software. The 1st design represents the conventional Schmitt TRIGGER with the transistor ratio proposed by (Wang *et al*., 1997). The 2nd design represents the design where the transistor ratio is kept as per this proposed design. The 3rd design is the proposed Schmitt trigger. The respective transistor dimensions for the three designs are shown in Table 1. The comparison is made in term of propagation delay.

**Table 1:** The Transistor Dimension

| $\frac{W}{L_{eff}}$ | 1st Design | 2nd Design | 3rd Design |
|---|---|---|---|
| P1 | $\frac{1.44}{0.18}$ | $\frac{1.08}{0.18}$ | $\frac{0.54}{0.18}$ |
| P2 | $\frac{1.44}{0.18}$ | $\frac{1.08}{0.18}$ | $\frac{0.54}{0.18}$ |
| P3 | $\frac{0.18}{0.18}$ | $\frac{0.54}{0.18}$ | $\frac{0.54}{0.18}$ |
| N1 | $\frac{1.8}{0.18}$ | $\frac{0.36}{0.18}$ | $\frac{0.36}{0.18}$ |
| N2 | $\frac{1.8}{0.18}$ | $\frac{0.36}{0.18}$ | $\frac{0.36}{0.18}$ |
| N3 | $\frac{1.44}{0.18}$ | $\frac{0.18}{0.18}$ | $\frac{0.18}{0.18}$ |

The proposed design is tested at 0.8, 1.0, 1.2 and 1.5V. The compilation of the simulation result is shown in Fig. 4.

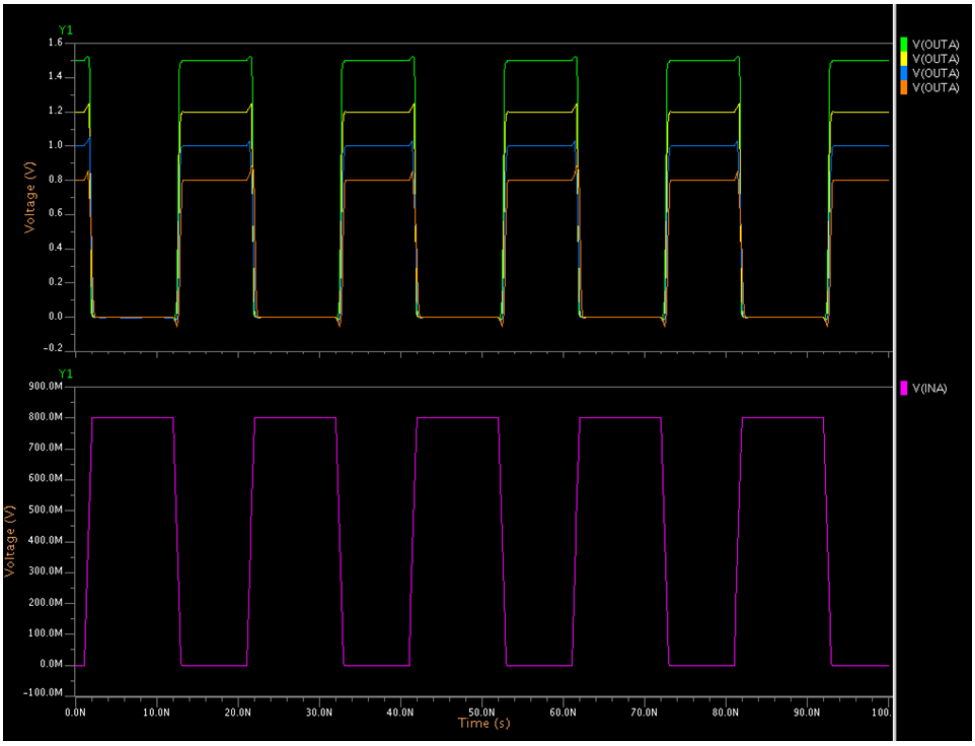


**Fig. 4:** Compilation of simulation results at various voltages

The result as shown in Fig. 4 shows that the proposed Schmitt Trigger can be successfully operated and can be used in low source voltage operation condition. The propagation delays are less in high voltage source compared to low voltage due to the transistor effective resistance and wire.

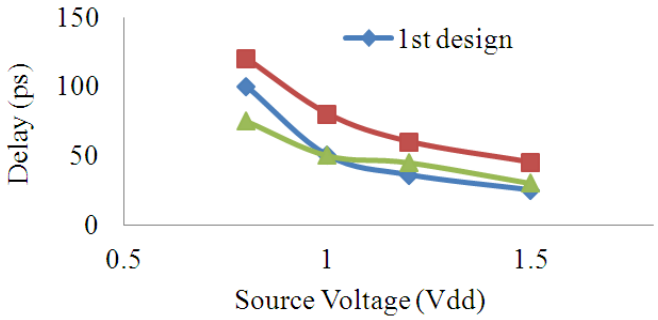


**Fig. 5:** Comparison of propagation delay

The comparison of the propagation delay between the designs is showed in Fig. 5. These results show that the proposed design is the best design in low source voltage in terms of propagation delay. The layout design is shown in Fig. 6.

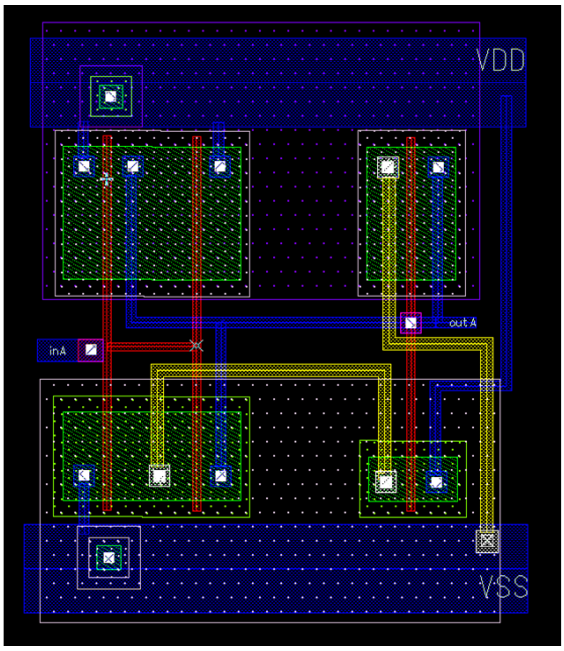


**Fig. 6:** Layout of the proposed Schmitt Trigger

*Conclusion:*

A new CMOS Schmitt trigger is presented in this study. The proposed design is capable to function at as low as 0.8 voltage. The circuit offers less propagation delay compared to the conventional circuit. It can be widely used in various low voltage analogue and digital applications.

**References**

Akter, M., M.B.I. Reaz, F. Mohd-Yasin and F. Choong, 2008. A modified-set partitioning in hierarchical trees algorithm for real-time image compression. J. Commun. Technol. Electronics, 53: 642-650.

Akter, M., M.B.I. Reaz, F. Mohd-Yasin and F. Choong, 2008. Hardware implementations of an image compressor for mobile communications. J. Commun. Technol. Electronics, 53: 899-910.

Chavez, S.R., 1995. Mixed-Mode Schmitt Trigger Equivalent Circuit. Electronics Letters, 31(3): 152-154.

Dejhan, K., P. Tooprakai, T. Rerkmaneewan and C. Soonyeekan, 2004. A high-speed direct bootstrapped CMOS Schmitt trigger circuit. In the proceedings of the IEEE International Conference on Semiconductor Electronics, pp: 68-71.

Filanovsky, I.M. and H. Baltes, 1994. CMOS Schmitt trigger design. Circuits and Systems I. IEEE Trans. Fundamental Theory Appl., 41: 46-49.

Kader, W.M., H. Rashid, M. Mamun. and M.A.S. Bhuiyan, 2012. Advancement of CMOS Schmitt Trigger Circuits, Modern Applied Science, 6(12): 51-58.

Kuang, J.B., and C.T. Chuang, 2001. PD/SOI CMOS Schmitt trigger circuits with controllable hysteresis. IEEE Int. Symp. VLSI Technology and Systems Applications, pp: 283-285.

Kulkarni, J.P. and K. Roy, 2012. Ultralow-voltage process-variation-tolerant schmitt-trigger-based SRAM design. IEEE Trans. Large Scale Integration Syst., 20: 319-332.

Lotze, N. and Y. Manoli, 2012. A 62mV 0.13µm CMOS Standard-cell-based design technique using schmitt-trigger logic. In the Proc. IEEE J. Solid-State Circuit, 47: 47-60.

Marufuzzaman, Mohd., M.B.I. Reaz, M.S. Rahman and M.A.M. Ali, 2010. Hardware prototyping of an intelligent current dq PI controller for FOC PMSM drive. In the proceedings of 6th International Conference on Electrical and Computer Engineering, pp: 86-88.

Mogaki, S., M. Kamada, T. Yonekura, S. Okamoto, Y. Ohtaki and M.B.I. Reaz, 2007. Time-stamp service makes real-time gaming cheat-free. In the proceedings of the 6th ACM SIGCOMM Workshop on Network and System Support for Games, Net Games, pp: 135-138.

Mohd-Yasin, F., A.L. Tan and M.B.I. Reaz, 2004. The FPGA prototyping of iris recognition for biometric identification employing neural network. In the proceedings of the International Conference on Microelectronics, pp: 458-461.

Reaz, M.B.I. and L.S. Wei, 2004. Adaptive linear neural network filter for fetal ECG extraction. In the proceedings of the International Conference on Intelligent Sensing and Information Processing, pp: 321-324.

Reaz, M.B.I., F. Chong and F. Mohd-Yasin, 2006. VHDL Modeling for classification of power quality disturbance employing wavelet transform. Artificial Neural Network Fuzzy Logic, Simulation, 82: 867-881.

Reaz, M.B.I., F. Choong, M.S. Sulaiman and F. Mohd-Yasin, 2007. Prototyping of wavelet transform, artificial neural network and fuzzy logic for power quality disturbance classifier. Electric Power Compo. Syst., 35: 1-17.

Reaz, M.B.I., F. Mohd-Yasin, S.L. Tan, H.Y. Tan and M.I. Ibrahimy, 2005. Partial encryption of compressed images employing FPGA. In the proceedings of IEEE International Symposium on Circuits and Systems, pp: 2385-2388.

Reaz, M.B.I., M.I. Ibrahimy, F. Mohd-Yasin, C.S. Wei, M. Kamada, 2007. Single core hardware module to implement encryption in TECB mode. Informacije MIDEM, 37(3): 165-171.

Reaz, M.B.I., M.T. Islam, M.S. Sulaiman, M.A.M. Ali, H. Sarwar and S. Rafique, 2003. FPGA realization of multipurpose FIR filter. In the proceedings of Parallel and Distributed Computing, Applications and Technologies, pp: 912-915.

Romli, N. B., M. Mamun, M. A. S. Bhuiyan, and H. Husain, 2012. Design of a Low Power Dissipation and Low Input Voltage Range Level Shifter in Cedec 0.18-µm CMOS Process, World Applied Sciences Journal, 19(8): 1140-1148.

Sapawi, R., R.L.S Chee, S.K Sahari and N. Julai, 2008. Performance of CMOS Schmitt Trigger. In the proceedings of the International Conference on Computer and Communication Engineering, pp: 1317-1320.

Schmitt, O. H., 1938. A thermionic trigger. J. Sci. Insrrum., 15(7): 24-26.

Singhanath, P., A. Suadet, A. Kanjanop, T. Thongleam, S. Kuankid and V. Kasemsuwan, 2011. Low voltage adjustable CMOS Schmitt trigger. In the proceedings of 4th International Conference on Modeling, Simulation and Applied Optimization, pp: 1-4.

Wang, C.S., S.Y. Yuan and S.Y. Kuo, 1997. Full-swing BiCMOS Schmitt trigger. In the Proceedings of the IEE Proc. Circuits, Dev. Syst., 144(5): 303-308.

Yuan, F., 2009. Current Regenerative Schmitt Triggers With Tunable Hysteresis. In the proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS '09), pp: 110-113.