Journal of Applied Science and Agriculture, 8(7) December 2013, Pages: 1079-1085

AENSI Journals

Journal of Applied Science and Agriculture

Journal home page: www.aensiweb.com/jasa/index.html

Programmable Current Mode Sensor Interface System for Biomedical Implantable Applications

[1]Saed Moradi, [1]Esmaeel Maghsoudloo, [2]Ehdieh Khaledian, [3]Abdorrasoul Ghasemi, [4]Azamossadat Nourbakhsh

[1]*Ferdowsi University of Mashhad, Faculty of Engineering, Electrical Engineering Department, 9177948974, Mashhad, I. R. Iran.*
[2]*University of Isfahan, Faculty of Engineering, Department of Computer Engineering, 8174673441, Isfahan, I. R. Iran.*
[3]*Islamic Azad University, Bushehr Branch, Department of Electrical Engineering, 7519619555, Bushehr, I. R. Iran.*
[4]*Islamic Azad University, Lahijan Branch, Department of Computer Engineering, 4416939515, Lahijan, I. R. Iran.*

ARTICLE INFO

Article history:
Received 14 October 2013
Received in revised form 26 November 2013
Accepted 28November 2013
Available online 25 February 2014

Keywords:
Biomedical Instrument
Sensor Interface
Current Mode
Analog To Digital Converter
0.18µm Cmos Technology

ABSTRACT

Background: Advances in CMOS technology, communications, and low power architectures have spurred considerable interest in implantable biomedical devices. The sensor interface is one of the critical building blocks in an implantable device. The main challenge in design of biomedical sensor interfaces is the nature of physiological signals. The amplitude range of physiological signals varies between 50 - 500 µV with frequency bandwidth from 0.1 Hz to 500 Hz. Therefore, low noise design is the major concern in developing of biomedical sensor interfaces. **Objective:** To design a low-voltage low-power high-performance biomedical sensor interface. **Results:** The input signal range is 0-5mV and the acceptable signal frequency range is from 0.1Hz to 500Hz. The resolution of the current mode successive approximation analog to digital converter is 8 bit. The circuit is simulated in 0.18µm CMOS technology with supply voltage of 1.8 V. At 40 Ks/S sampling frequency, the total power consumption and total harmonic distortion of the system are obtained 2.2 µW and -45.2 dB respectively. **Conclusion:** A low power current mode circuit is presented for biomedical sensor interface applications. An adaptable band- pass filter is used in front end of the system for providing flexibility in its passband for different biomedical applications. The Gm and current mode SAR ADC are designed in a way to achieve minimum power consumption. The simulation results demonstrated the effectiveness and superiority of the proposed circuit in comparison with the conventional circuits.

To Cite This Article: Saed Moradi, Esmaeel Maghsoudloo, Ehdieh Khaledian, Abdorrasoul ghasemi, Azamossadat Nourbakhsh., Programmable Current Mode Sensor Interface System for Biomedical Implantable Applications. ***J. Appl. Sci. & Agric.,*** *8(7): 1079-1085, 2013*

INTRODUCTION

Advances in CMOS technology, communications, and low power architectures have spurred considerable interest in implantable biomedical devices. The sensor interface is one of the critical building blocks in an implantable device. The main challenge in design of biomedical sensor interfaces is the nature of physiological signals. The amplitude range of physiological signals varies between 50 - 500 µV with frequency bandwidth from 0.1 Hz to 500 Hz. Therefore, low noise design is the major concern in developing of biomedical sensor interfaces (Li, Dong *et al*. 2010, Vuorela, Seppa *et al*. 2010).

To capture small bio-potential changes accurately, the sensor interface has to incorporate a low noise amplifier with sufficient gain, a band-pass filter to reduce the DC offset and noise of input signal and an analog to digital converter (ADC) with a resolution greater than or equal to 8 bits (Długosz and Iniewski 2007). Also, to increase the battery life of the implantable system, the power consumption of the circuits should be minimized (Li, Poon *et al*. 2010).

A few researches have been dedicated to improve the performance of the system. A low-noise amplifier with adjustable gain and bandwidth was presented in (Yin and Ghovanloo 2007). A low-noise low-power single-ended operational trans conductance amplifier (OTA) with capacitive feedback for neural recording applications is described in (Harrison and Charles 2003). Another low-power bio-signal interface that consumes 2.3 µW at 1 V supply was introduced in (Zou, Xu *et al*. 2009) in which it employs two amplifiers to optimize the power efficiency.

In this work a current mode approach is used to improve the power consumption and total harmonic distortion (THD) of the system.

Corresponding Author: Saed Moradi, Ferdowsi University of Mashahd, Integrated Systems Lab. (ISL), 9177948974, Mashhad, I.R. Iran.
Phone: +989359768847, E-mail: saed.moradi@gmail.com

Journal of Applied Science and Agriculture, 8(7) December 2013, Pages: 1079-1085

This paper is organized as follow: Section 2 describes the system architecture of the low power sensor interface. Design procedure for the circuits is introduced in section 3. Section 4 presents the simulation results of the circuits and system and finally section 5 provides conclusion.

System Architecture:

In this section the architecture of current-mode interface for biomedical applications is described. As shown in Fig. 1, the block diagram of this system includes a low noise amplifier (LNA) (Yin and Ghovanloo 2007), an operational transconductance amplfier (Gm) and a current -mode successive approximation (SAR) ADC. The advantages of current mode SAR ADC in comparison with voltage mode are its lower power consumption, lower noise, lower chip area and using capacitor-less digital to analog converter (DAC). The circuit architecture of each block must be designed in a way to be compatible to other blocks.

As illustrated in Fig. 1, a band-pass filter amplifies the input signal and filters unwanted frequency bands to decrease noise level. The common mode of the OTA's input signal is tuned in a way to achieve maximum linearity range of Gm. The OTA converts the amplified voltage signal to current. This current is converted to digital codes using a current mode SAR ADC. The binary-weighted current source array serves as digital-to-analog converter (DAC) (Długosz and Iniewski 2007).

Circuit Design:

Front-End Amplifier:

The proposed filter's schematic is shown in Fig. 2-a. To increase the flexibility of the interface system for different physiological signals, passband of the filter is variable. The lower cut-off frequency is determined by feed-back resistance between 0.01 Hz - 10 Hz which in turn is defined by gate voltages (V_n and V_p) of pseudo-resistors M_n and M_p. Two diode-connected transistors are used to achieve big resistance with small area size (Harrison and Charles 2003). In this way, the value of the resistance can reach 6.36 TΩ. A biasing circuit adjusts the gate voltages of M_n and M_p (Fig. 2, b).Variation of current of transistor M_1 in biasing circuit results in changing of V_n and V_p. Load capacitance of the filter dictates the upper cut-off frequency between 100 Hz – 1 kHz.

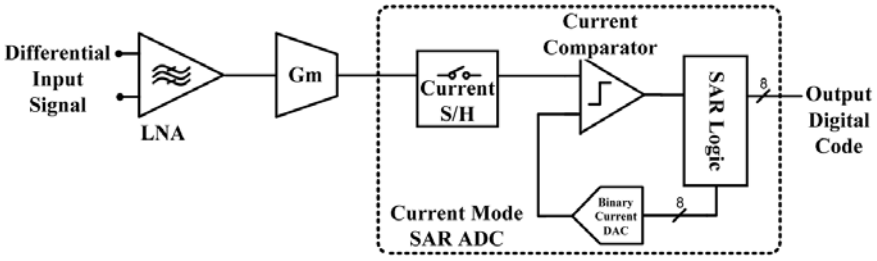


Fig. 1: Current mode sensor interface outline.

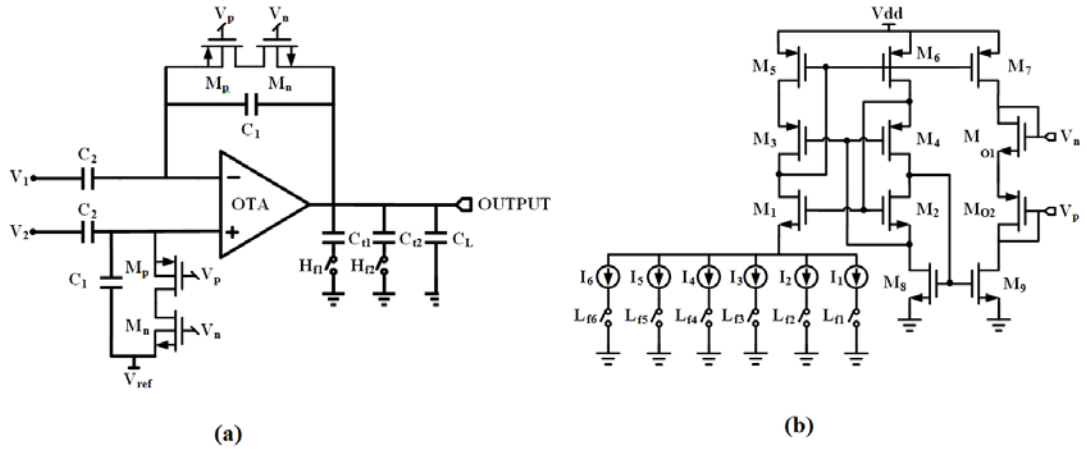


Fig. 2: (a) Schematic of OTA– based front-end amplifier with capacitive feed-back, (b) the biasing circuit for pseudo resistor.

Journal of Applied Science and Agriculture, 8(7) December 2013, Pages: 1079-1085

Operational Transconductance Amplifier:

Operational transconductance is an active element that is used to convert the input voltage to current. Fig. 3 shows a cascaded current-mirror OTA that is used in this paper (Harrison and Charles 2003). Using both NMOS and PMOS transistors as the input of the OTA increases common mode voltage range of the input signal and hence improve linearity of the system. Also a pre-amplifier with higher gain can be used to decrease the effect of noise on the input signal of the OTA, without degradation in linearity of the system. Adaptable gain of OTA is provided by changing in biasing current to match maximum input current of the next stage with different input signals.

Analog-to-Digital Converter:

A generic structure of the current SAR ADC is illustrated in Fig. 4. In convert mode, current sample and hold circuit (S/H) holds the input current and a current comparator compares it with generated current of digital to analog converter (DAC). The output of the comparator specifies output bits of logic circuit. These bits determine the DAC current level for comparison at the next cycle. After 9th operating cycle, the output digital code is obtained.

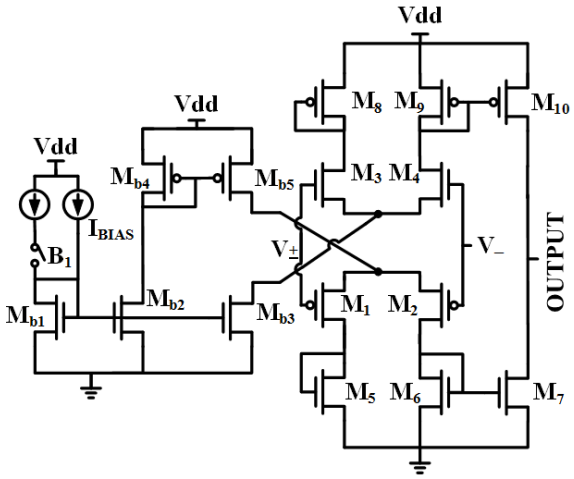


Fig. 3: Schematic of operational transconductance Gm.

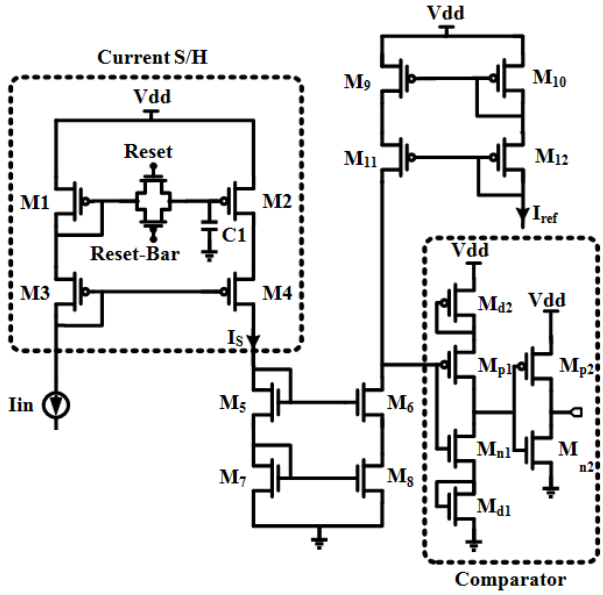


Fig. 4: Schematic of the S/H and comparator circuit of the ADC.

As shown in Fig. 4, when the transmission gate is closed, the circuit is at track phase in which I_S tracks I_{in}. In holding mode, the transmission gate is open and I_S holds the constant value of I_{in}. This value depends on charge of C1 at the tracking mode. The critical problem in this S/H circuit is reduction of voltage on C1 due to the leakage current in the transmission gate. Effect of the leakage current can be decreased by increasing size of C_1. But choosing big capacitors results in higher power consumption and larger chip area. Therefore, there is a compromise between the power consumption, area and accuracy of the S/H. The conventional current

comparator circuit utilizes two cascaded inverters. The input current collects in gate-source capacitance of first inverter, so the input and output voltage of the inverter is dependent on difference between I_S and I_{ref}. Second inverter produces the logical level for using in the register circuit. To reduce the power consumption of the comparator when difference between the input current and the reference current is low, two diode connected transistors are added to conventional current comparator (Fig. 4). Therefore, drain-source voltages of M_{p1} and M_{n1} are reduced to decrease the first inverter current.

In this current mode ADC, cascode current mirrors are used to obtain high output impedance. But, using this topology reduces the voltage swing and hence, lower current could be mirrored in this design. Also, to decrease the mismatch between threshold voltage of P-type and N-type transistors, two kinds of current mirrors (P-type and N-type) are used (Fig. 4).

In this work, a current-mode digital-to-analog converter (DAC) is utilized (Fig. 5). The DAC current is produced by mirroring the reference current I_{DAC}. The LSB current (I_{LSB}) is 500pA, so quantization levels are 0.5nA, 1nA, 2nA, 4nA, 8nA, 16nA, 32nA and 64nA. Also, full scale current $I_{full\text{-}scale}$ is defined as:

$$I_{full-scale} = 2^{N+1}.I_{LSB} \quad (1)$$

therefore for this circuit, *Ifull-scale*=128nA.

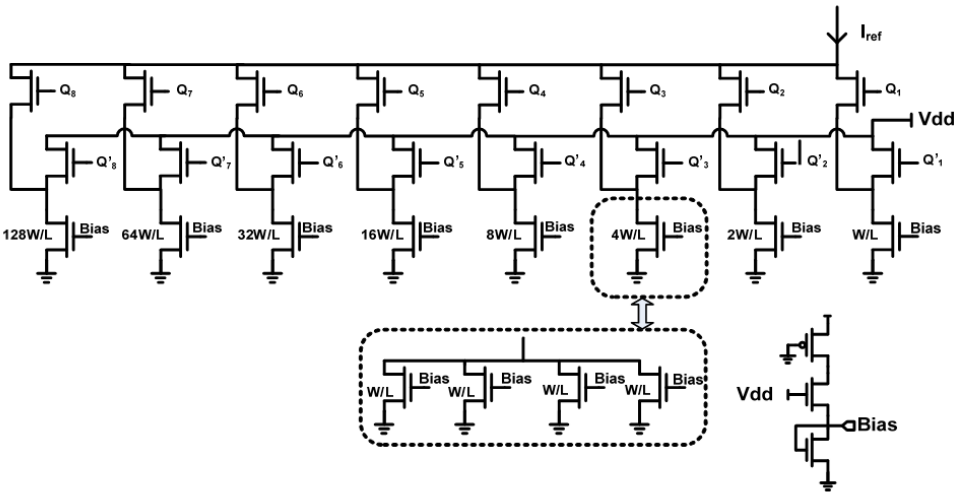


Fig. 5: Schematic of the binary-weighted current DAC.

Simulation results:

The proposed circuits are simulated using Hspice with standard TSMC 0.18µm CMOS technology in room temperature. Input signal range of this system is 0-5mV that covers biological signals such as EOG, EEG and ECG. The first block is a filter that amplifies the input signal to 0-50mV range. As shown in Fig. 6, typical value of the lower cut-off frequency and the higher cut-off frequency of the filter are 0.1 Hz and 500 Hz, respectively. Since 6 bits are provided to program the resistance of pseudo-resistors, 2^6 levels are available for the resistance between 3.18 GΩ and 6.36 TΩ and the lower cut-off frequency between 0.01 Hz and 10 Hz. Changing the output capacitance of the filter between 10 pF and 200 pF results in variation of higher cut-off frequency in the range of 100 Hz to 1 KHz.

Journal of Applied Science and Agriculture, 8(7) December 2013, Pages: 1079-1085

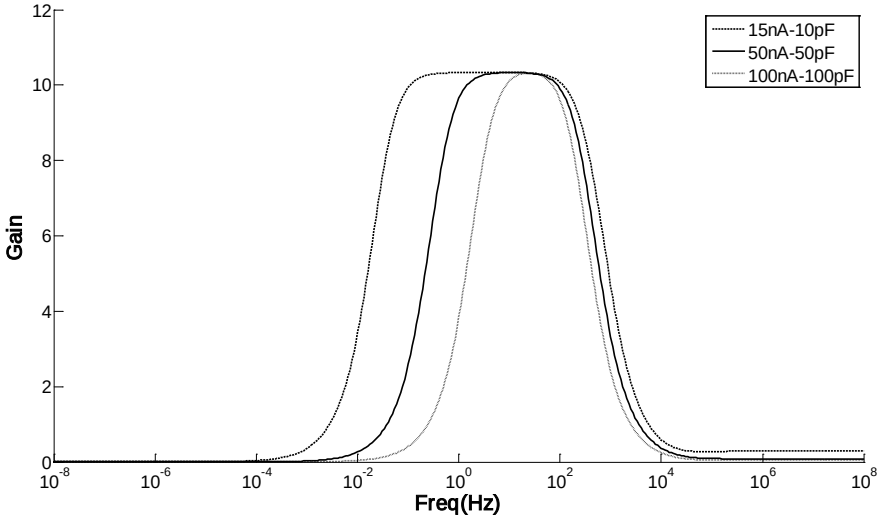


Fig. 1: Frequency response of the front-end amplifier.

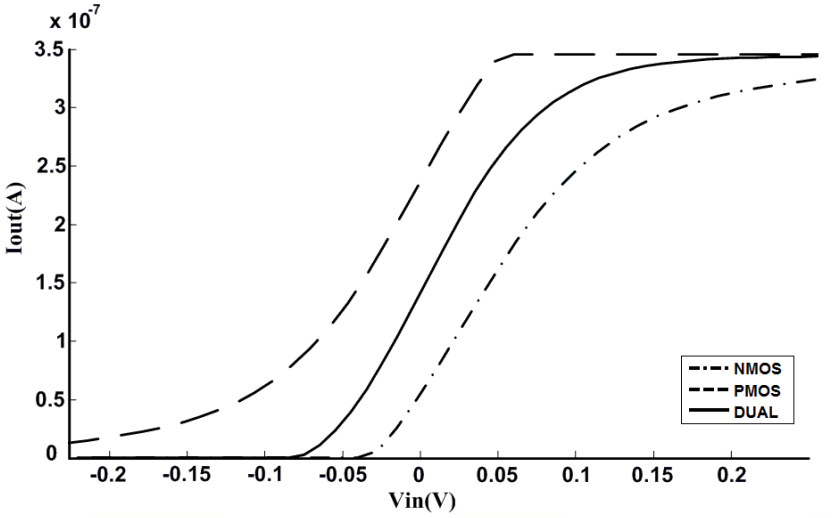
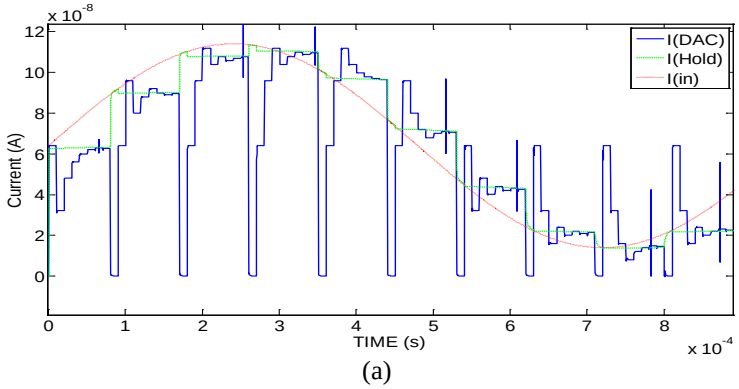


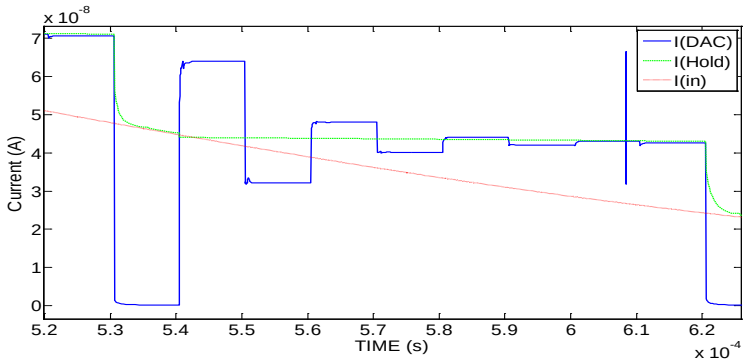
Fig. 7: Simulated result of the operational transconductance Gm.

The simulation results show improvement in the linearity of the proposed Gm circuit. Maximum linearity range of the Gm circuit is obtained in the range of -75 mV to +75 mV (Fig. 7). Transconductance value of this circuit is 2.57µA/V. The simulation results indicate that LSB current (ILSB) equals 500pA. Also other quantization levels are 0.5nA, 1nA, 2nA, 4nA, 7.97nA, 16.01nA, 32.04nA and 64.07nA that are close to desirable values. As shown in Fig. 8-a, the S/H circuit tracks and samples the input signal near both the full scale and zero levels. The ADC determines the full scale input signal levels after 9 clocks with error less than 1 LSB (Fig. 8-b).



(a)

Journal of Applied Science and Agriculture, 8(7) December 2013, Pages: 1079-1085



(b)

Fig. 8: (a) Performance of SAR ADC, data frequency is 10 KHz, (b) successive tracking for I_{in}=42 nA.

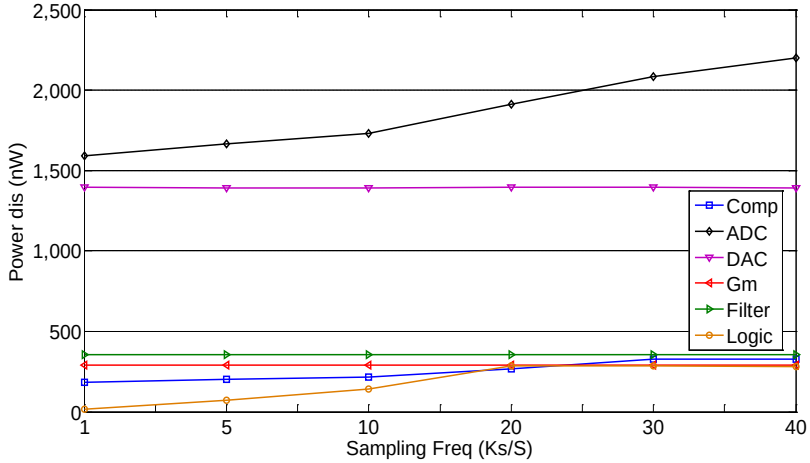


Fig. 9: The power consumption of the interface blocks versus the sampling frequency.

Fig. 9 shows the simulation results of the power consumption of different blocks of the interface circuit versus the sampling frequency. Whereas the power consumption of Gm, filter and DAC circuits are constant with sampling frequency, the power consumption associated with the logic circuit and comparator, hence the ADC power consumption rises as the sampling frequency increases. The specifications of the current mode SAR ADC is compared with a few SAR ADCs in table 1. The proposed circuit has superior performance, especially in comparison with voltage mode SAR ADCs. Figure of merit of the proposed ADC, defined as the ratio of the sampling frequency to the power consumption is 4.65 MHz/µW. Table 2 represents THD of the system in process variation corners. Effective number of bit (ENOB) at TT point is 7.21 bits.

Table 1: Comparison of Performance of Some Low Power SAR ADCs.

	CMOS process (µm)	Resolution	Fs (KHz)	Power Diss. (µW)	Mode	VDD (V)	FOM (MHz/µW)
(Lee and Song 1999)	0.6	8	100	980	V	3	0.03
(Agarwal, Kim *et al*. 2005)	0.18	6	125	6	I	0.65	1.33
(Długosz and Iniewski 2007)	0.18	8	2000	0.56	I	0.55	0.035
(Scott, Boser *et al*. 2003)	0.25	7	100	3.1	V	1	4.13
This work	0.18	8	40	2.2	I	1.8	4.65

Table 2: Simulation results of THD at process corners.

Process Corners	THD (dB)
TT	-45.2
FF	-43.3
SS	-40.08
FS	-44.12
SF	-39.83

Conclusion:

A low power current mode circuit is presented for biomedical sensor interface applications. An adaptable band- pass filter is used in front end of the system for providing flexibility in its passband for different biomedical applications. The Gm and current mode SAR ADC are designed in a way to achieve minimum

power consumption. The simulation results proved that the circuit can work with the input signal range from 0-5mV and the signal frequency range from 0.1Hz to 500Hz. The figure of merit and ENOB of the ADC are 4.65 MHz/µW and 7.21 bits, respectively. The power consumption of proposed system with supply voltage of 1.8V and sampling frequency of 40Ks/S is 2.2µW.

REFERENCES

Agarwal, A., Y. Kim and S. Sonkusale (2005). Low power current mode ADC for CMOS sensor IC. Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on, IEEE.

Długosz, R. and K. Iniewski (2007). "Flexible architecture of ultra-low-power current-mode interleaved successive approximation analog-to-digital converter for wireless sensor networks." VLSI Design 2007.

Harrison, R. R. and C. Charles (2003). "A low-power low-noise CMOS amplifier for neural recording applications." Solid-State Circuits, IEEE Journal of 38(6): 958-965.

Lee, J. and M. Song (1999). Design of an 8-bit 100 KSPS 1 mW CMOS A/D converter for digital mobile communication. ASICs, 1999. AP-ASIC'99. The First IEEE Asia Pacific Conference on, IEEE.

Li, B., M. Dong and M. Vai (2010). "Modelling cardiovascular physiological signals using adaptive Hermite and wavelet basis functions." IET signal processing 4(5): 588-597.

Li, Y., C. C. Poon and Y.-T. Zhang (2010). "Analog integrated circuits design for processing physiological signals." Biomedical Engineering, IEEE Reviews in 3: 93-105.

Scott, M. D., B. E. Boser and K. S. J. Pister (2003). "An ultralow-energy ADC for smart dust." Solid-State Circuits, IEEE Journal of 38(7): 1123-1129.

Vuorela, T., V.-P. Seppa, J. Vanhala and J. Hyttinen (2010). "Design and implementation of a portable long-term physiological signal recorder." Information Technology in Biomedicine, IEEE Transactions on 14(3): 718-725.

Yin, M. and M. Ghovanloo (2007). A low-noise preamplifier with adjustable gain and bandwidth for biopotential recording applications. Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on, IEEE.

Zou, X., X. Xu, L. Yao and Y. Lian (2009). "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip." Solid-State Circuits, IEEE Journal of 44(4): 1067-1077.