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A Novel Multi-Mode quadrature Oscillator with Simple Structure and High Oscillation Frequency Using CCII

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ABSTRACT

Background: The oscillators is one of the most building block of many analog signal processing, communication and instrumentation systems that can provide dual voltage and current sinusoidal outputs for essential parts such as phase locked loops, clocks and sensors. The simple structure, high frequency oscillation, low power and low voltage feature and ability to produce quadrature sinusoidal signals with multi-mode structure, are main goals of oscillator design. The collection of these in unique configuration is one of the Meaningful and challenging works for analog circuit designer. **Objective:** To optimize frequency performance and power consumption with reduced circuit complexity and reduction in number of active and passive elements. **Results:** Compared with other same works, the proposed quadrature oscillator provides high frequency oscillation, low power consumption and good linearity. The circuit is exhibited the oscillation frequency about one hundred Mega-Hz and its THD is less of 1%. The circuit use from dual positive and negative supply voltages ± 0.75 Volt and its total power consumption is 2.4mWatt. As well as, the suggested structure presents multi-mode feature that can produce dual quadrature voltage and current outputs. **Conclusion:** We have proposed a multi-mode quadrature oscillator with new structure and new CCII (second generation current conveyor) as active element. The especial features of the proposed circuit are low complexity, low voltage, low power, good linearity and high oscillation frequency. The circuit can be used in multi-mode analog structure because it able to construct a quadrature voltage or current outputs. The presented circuit can be implemented by the parallel switch resistance that it cause to make various frequency oscillations about one hundred MHz.

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INTRODUCTION

In the first time, the basic structure of second generation current conveyor (CCII) was expanded by Sedra and Smith (A. Sedra, K. Smith, 1970). Current conveyors can be applied in voltage and current analog components but it can be better that be used from CCII as one of the basic active elements in multi-mode analog interfaces such as oscillators, filters and data converters.

Recently, one of the state of the art subjects in consideration of analog signal processing circuit designers is development in performance parameters of CCII circuits. The results of these investigations lead to resolution increasing in current and voltage transfer functions, compensation of offset (H. O. Elwan, A. M. Soliman, 1996), improvement in transfer functions linearity (G. Palmisano, G. Palumbo, S. Pennisi, 1999) and high frequency features (N. B. El Feki, S. B. Salim and D. S. Masmoudi, 2008) optimization circuit toward low power and low voltage design (H. O. Elwan, A. M. Soliman, 1997) and trend for differential circuitry. Among these goals, the features of the low power and low voltage circuit design, wide linearity range of CCII transfer functions and their high frequency response can be optimized for using them as basic active elements in analog signal processing and mobile communication structures such as oscillators and filters. The oscillators is one of the most building block of many analog signal processing, communication and instrumentation systems that can provide dual voltage and current sinusoidal outputs for essential parts such as phase locked loops, clocks and sensors. The quadrature oscillators using only all grounded passive elements are of special interest. QOs simultaneously provide two sinusoids which are 90° phase-shifted and have widespread applications in quadrature mixers and single-side band modulators (W. Tangsrirat, D. Prasertsom, T. Piyatat and W. Surakomponorn, 2008).

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The conventional op amp based RC active oscillators often product a low frequency oscillation with moderate linearity performance another disadvantage of them is high power consumption. To overcome these limitations active OTA-C circuit and current conveyor based oscillators are good alternative choices.as is reported in some recent literatures the CCII-based oscillators can be focus on some goals preferment such as high linearity and high frequency performances (Maheshwari, Sudhanshu, and RishabhVerma, 2012), simple configuration and low power consumption. however, these reported circuits often suffer from one or more disadvantages: (i) extra numbers of active and passive elements (M. Kumngern, B. Knobnob, and K. Dejhan, 2009) (S. Maheshwari and I. A. Khan, 2006),(ii) using floating capacitors (S. Maheshwari, 2004),(iii) use of floating resistors that can be pressed the percent of error and employing of moderate oscillation frequency (Horng, Jiun-Wei, Zhao-Ren Wang, and Tun-Yi Yang, 2011). (V) Don't have multi-mode structure. In this paper, we have designed a quadrature oscillator that doesn't suffer any of noted disadvantages.

Objectives:

In this paper, at the first the classical unity gain current conveyor with symmetric current direction in output nodes is presented. The parameters of linearity boundary, frequency response and low voltage requirements have been improved in comparison with other same works. Moreover, another advantage of offered circuit is the simple and differential structure. In continuation of paper, a new multi-mode quadrature oscillator with simple structure and high oscillation frequency using translinear current conveyors was designed. The presented structure use from two CCII, two capacitors and two resistors and it have multi-mode configuration that can be product a quadrature sinusoid current and voltage outputs about one hundred of MHz frequency. The linearity of circuit is illustrated with harmonic analysis and result was shown in simulation result, furthermore the performance parameters such as delay time, frequency oscillation and amplitude were evaluated by changing resistance and total harmonic distortion (THD) was calculated to prove the high linearity performance.

MATERIAL AND METHODS

The Proposed CCII Circuit:

Current conveyors are basic and applied active components in analogue interfaces and elementary signal processing cells especially with the current mode configuration. Basic construction of ideal CCII is formed by three ports, x, y and z. The model of CCII can be introduced negative or positive styles with regard to output current direction at node z. the direction of output current can be internal or external. Figure 1 shows the blocked style of dual positive and negative implementation.

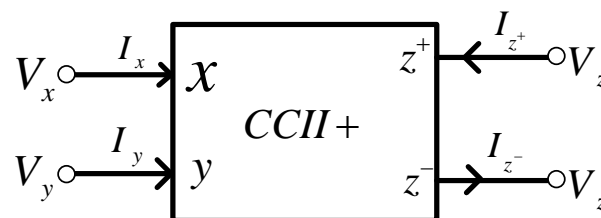


Fig. 1: the block diagram scheme of the positive CCII

The CCII can be explained by two sub-circuits: voltage follower and current-mirror. Gains of current mirror and voltage follower are one in the unity gain CCII. As a result, equations of unity gain dual output current nodes type of CCII can be given by (P. S. Manhas, K. pal, S. Sharma, L. K. Mangotra, K. K. S. jamwal, 2009):

$$V_x = V_y + R_x I_x, I_y = 0, I_x = I_{z^-} = I_{z^+} \quad (1)$$

Currents and voltages that are applied in above equations have distinguished in schematic of figure 1 and R_x is parasitic resistance at node x.

The offered circuit of CCII is shown in the figure 3. Its dimensions are optimized for high frequency and can be used in RF analog structures. The proposed circuit is implemented in the standard 0.18 μ m CMOS TSMC technology. Furthermore its configuration presents low voltage, rail to rail and high linearity features. Therefore dual differential pair of PMOS and NMOS transistors has been chosen for the input stage (M8, M9, M10 and M11) that can provide the rail to rail specification. As Figure 3 shows, transistors M8 and M11 prepare the input positive amplitude however the transistors M9 and M10 prepare the negative one. in this design active load of voltage follower stage is created by NMOS transistors (M14, M15) and PMOS transistors (M2, M4) as current mirrors consequently, the bias currents in dual lines of voltage follower stage are equal and it lead to same voltages at nodes x and y.

As shown in Figure 3, For equalization current at node x and current at node z^+ are used from current mirrors M5, M6, M16, M17 and for the same currents with opposite direction at node z^- are used from current mirrors M18, M19, M20, M21, M22, M23.

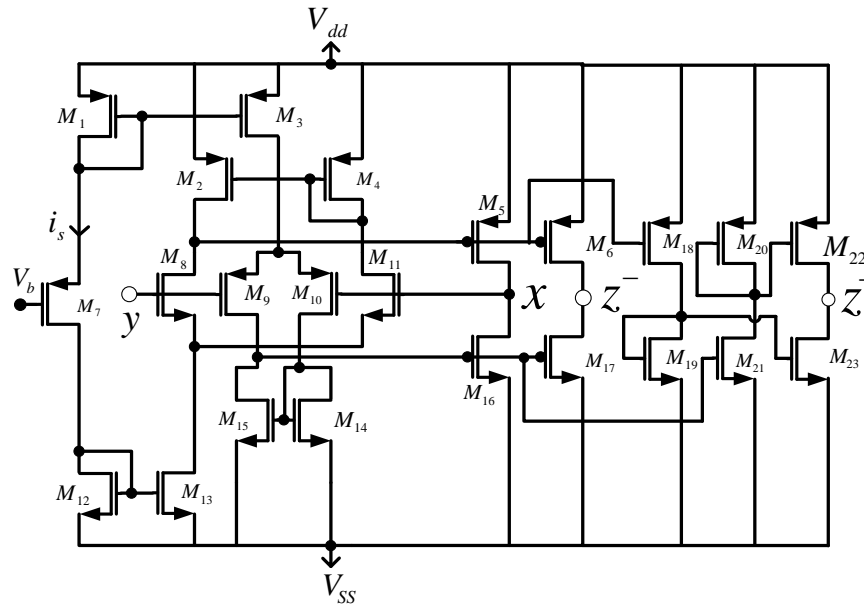


Fig. 3: The schematic of suggested CCII circuit

The proposed low voltage and high frequency CCII is simulated in the standard $0.18\mu\text{m}$ CMOS TSMC technology. The HSPICE software has used for simulation and the used dimensions of CMOS transistors has been set in the table 1. The suggested CCII is composed of dual symmetric supply voltages $\pm 0.75\text{V}$ that is indicated the low voltage characteristic. Figure 5 shows the linear relation between terminals x and y which identify the linearity specification of voltage transfer function. As shown in this figure, voltage in node x tracks the voltage in node y from -0.7V to $+0.7\text{V}$ with linear curvature as a result, the rail to rail dynamic range of voltage variation can be employed.

Figure 6 shows the linear relation between internal and external output current of terminals z^+ and z^- versus the internal current of terminal x . these current transfer functions prove the capability of current drive in output stage of proposed CCII, because of the unity gain design, the voltage and current transfer function curves according to the Figures 5 and 6 have unit slope which their variation errors are less of 1%.

Table 1: the dimensions of CMOS transistor of proposed CCII

Transistors	W/L($\mu\text{m} / \mu\text{m}$)
M12	(0.5/0.18)
M14,M15	(1/0.18)
M1	(1.5/0.18)
M8,M11	(2/0.18)
M2,M4	(3/0.18)
M16,M17,M19,M21,M23	(4/0.18)
M9,M10	(6/0.18)
M5,M6,M18,M20,M22	(12/0.18)
M1	(24/0.18)
M7,M13	(30/0.18)
M3	(90/0.18)

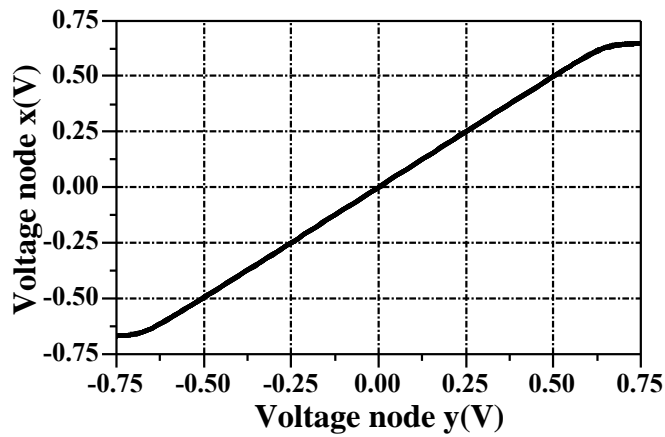


Fig. 5: the voltage at node x versus the input voltage of node y

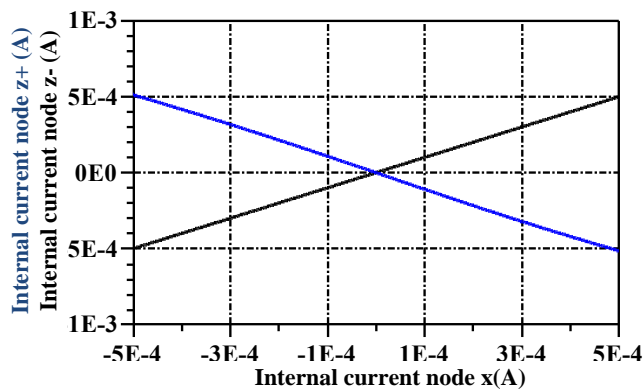


Fig. 6: the output currents at terminals z^+ and z^- versus internal current of terminal x

In this proposed circuit the -3dB cut-off frequencies for voltage and current transfer functions are 3.87GHz and 3.23GHz respectively. The specific of high frequency performances of proposed CCII can able it for using in analog RF components.

The Proposed CCII-based Oscillator:

Recently, oscillators that operate in the low-power and high frequency are one of the important basic building blocks of analog components. Phase shift oscillators have been used more than single phase oscillator. A quadrature oscillator is a special type of phase shift oscillator that produces two sine-spectrums with 90° deference phase. A multi-mode quadrature oscillator can produce voltage and current output and can be used in multi-mode analog structures. In this paper a multi-mode quadrature oscillator with novel and simple structure had been designed and simulated. Figure 7 shows the configuration with two resistors, tow capacitor and two CCII.

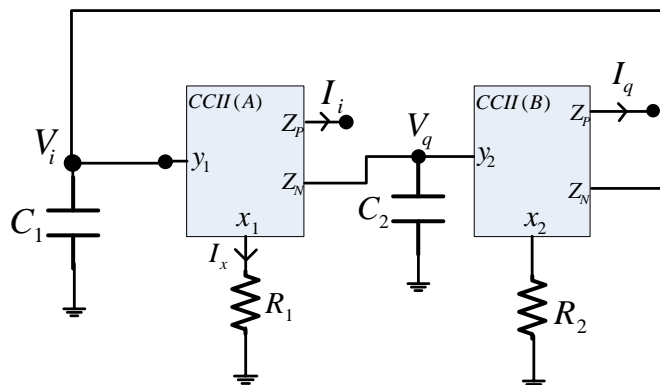


Fig. 7: the multi-mode quadrature oscillator scheme

This oscillator can create quadrature voltage oscillations in nodes V_i and V_q also quadrature current oscillations in nodes I_i and I_q . The oscillator because of use from four passive and two active elements and applying of simple and optimize CCII have low power and low complexity. Furthermore, the frequency oscillation can be high due to high frequency CCII features

For reaching a quadrature oscillation, two voltage oscillations based on following formula must be created at node V_i and V_q .

$$V_i = A_i \cos(\omega t) \quad (2)$$

$$V_q = A_q \cos(\omega t \pm 90) \quad (3)$$

The above equations can convert together by derivative operation ($V_i = \frac{d(V_q)}{dt}$). So the relation between quadrature voltage oscillations can be given by applying Laplace transformation as following:

$$V(S)_i = kSV_q(S) \quad (4)$$

If considering the relationships of equation (1), the reciprocal equations (5) and (6) can be given by applying Kirchhoff's current law (KCL) at nodes V_i and V_q shown in figure 7.

$$V_i(S) = SC_2(R_1 + R_{X1})V_q(S) \quad (5)$$

$$V_q(S) = -SC_1(R_2 + R_{X2})V_i(S) \quad (6)$$

As seen, the equations (5) and (6) are according to equation (4). Consequently, the phase difference between voltages V_i and V_q is 90° . As well as Laplace equation (7) can be obtained by replacing equation (5) in (6) as following:

$$(S^2C_1C_2(R_1 + R_{X1})(R_2 + R_{X2})) = -1(S = j\omega, S^2 = -\omega^2) \quad (7)$$

From resolving equation (7), the frequency oscillation can be given as follow:

$$\omega_{os} = \sqrt{\frac{1}{C_1C_2(R_1 + R_{X1})(R_2 + R_{X2})}} \quad (8)$$

According to equation (1) and by refer to figure 7, it can be seen that the current I_i have linear relation with voltage V_i and current I_q have linear relation with V_q . The relations, lead to construction of quadrature current I_i and I_q with same phase by V_i and V_q respectively. Furthermore, from equation (5) and (8) can be realized that the frequency and amplitude oscillation can be changed by variation of resistance R_1 and R_2 , so we can change them by use of digital switch and pins.

Result:

To verification of theoretical prediction of the proposed multi-mode oscillator, the circuit has been simulated using Hspice. The CMOS implementations of oscillator are using from $0.18\mu\text{m}$ TSMC CMOS technology parameters. The proposed circuit has 2.4mWatt power consumption at ± 0.75 power supply.

Figure 8 shows the quadrature output voltages and currents in two separate schemes. The selections of passive elements for recording quadrature voltage and current outputs are $R_1 = 850\Omega$, $R_2 = 500\Omega$, $C_1 = 2.7\text{pF}$ and $C_2 = 4\text{pF}$. The oscillation frequency is equal to 73MHz and THD (total harmonic distortion) is less of one percent that proves the linearity performances. The voltage and current amplitudes are different that it can be equal by Resistive divider circuit.

Fast Fourier transform (FFT) can be used with a MATLAB code and Output spectrum can be drawn for frequency evaluation of circuit. Figure 9 shows the power spectral density of voltage V_i . In this figure The Basic frequency and harmonic bins are visible.

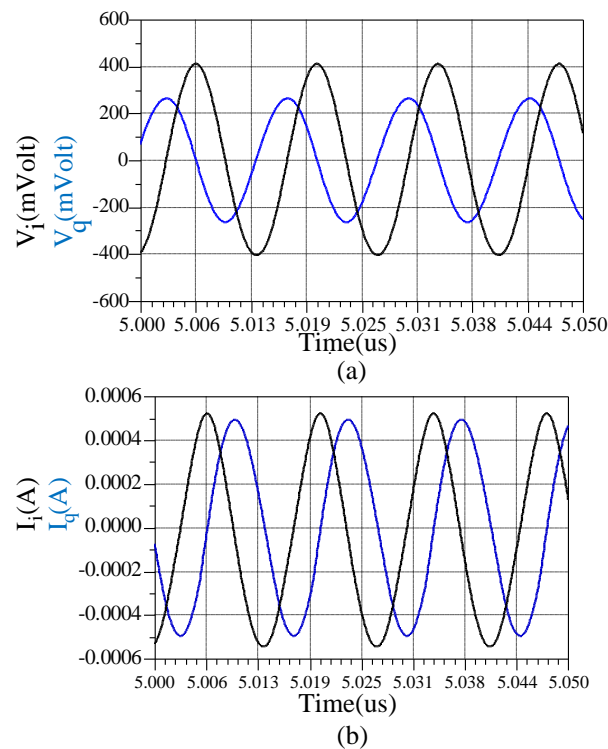


Fig. 8: (a) voltage outputs (b) current outputs of figure 7

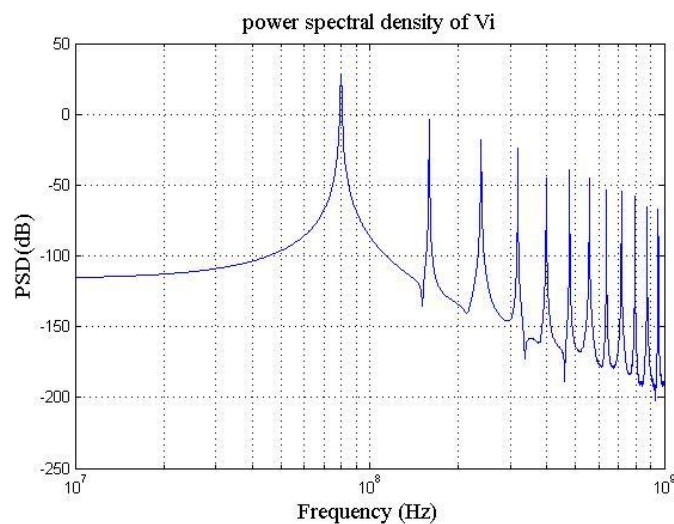


Fig. 9: power spectral density of voltage V_i

The proposed multi-mode quadrature oscillator use from two grounded resistances R_1 , R_2 and two grounded capacitances C_1 , C_2 . In this circuit, the oscillation condition and oscillation frequency can be orthogonally controllable by changing each other elements, so the various results of frequency oscillation, amplitudes, THD and delay time can be obtained by variation of resistor R_1 . Figure 10 shows the voltage and current output delay times by changing R_1 from 300Ω to 700Ω . It can be seen that the delay time was increased by increasing R_1 .

Figure 11 indicate the variation of frequency oscillation parameter by changing R_1 . As shown in this figure, there is an inverse relationship between frequency oscillation and size of resistance R_1 .

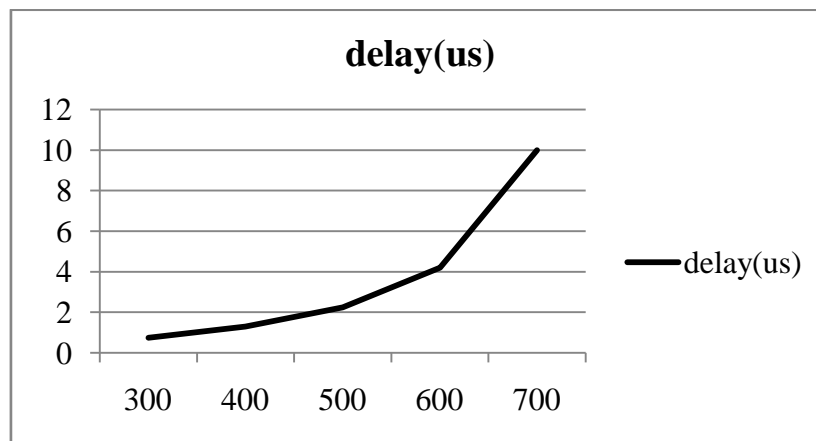


Fig. 10: the delay time versus change in resistance R_1

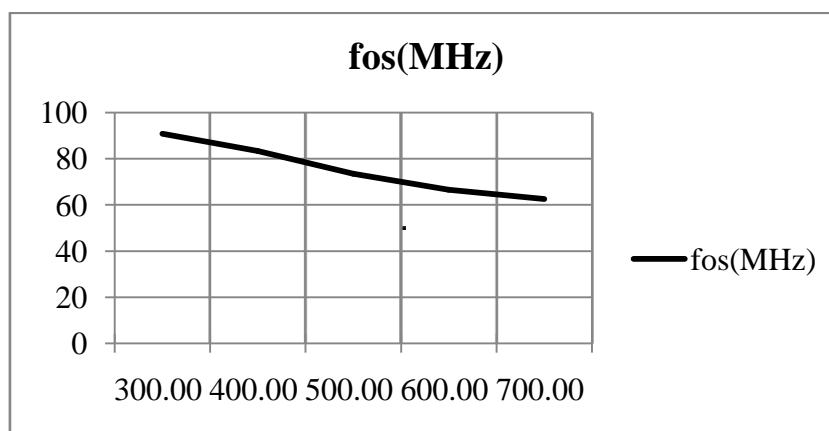


Fig. 11: the variation of oscillation frequency versus change in resistance R_1

Figure 12 and 13 show the amplitude variation of voltage and current outputs versus change in resistance R_1 , respectively. Figures show decreasing trend of quadrature current and voltage amplitudes rather than increasing of R_1 .

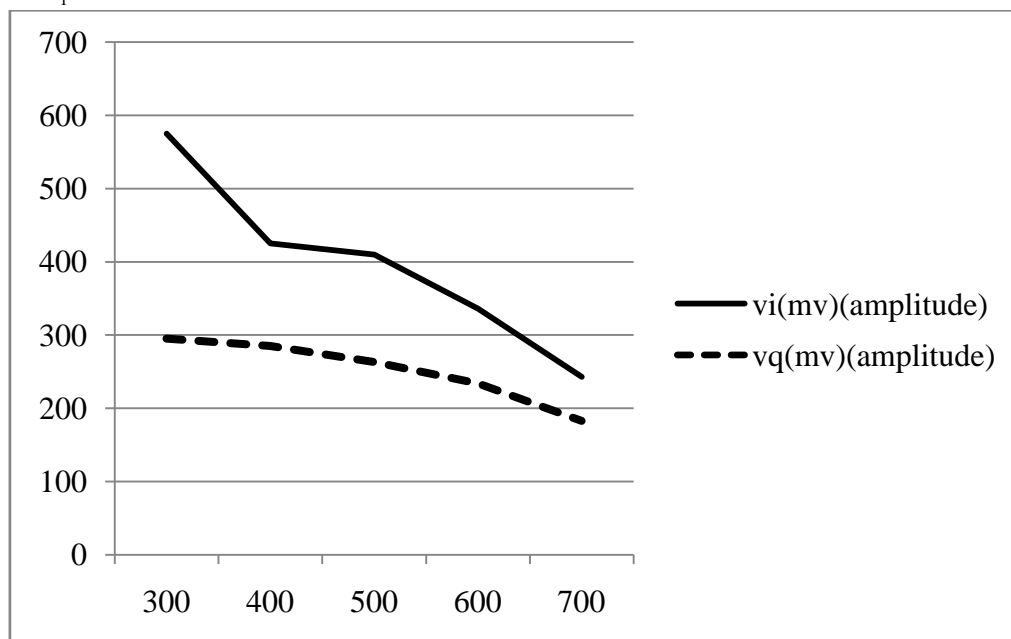


Fig. 12: the variation of voltage amplitudes versus change in resistance R_1

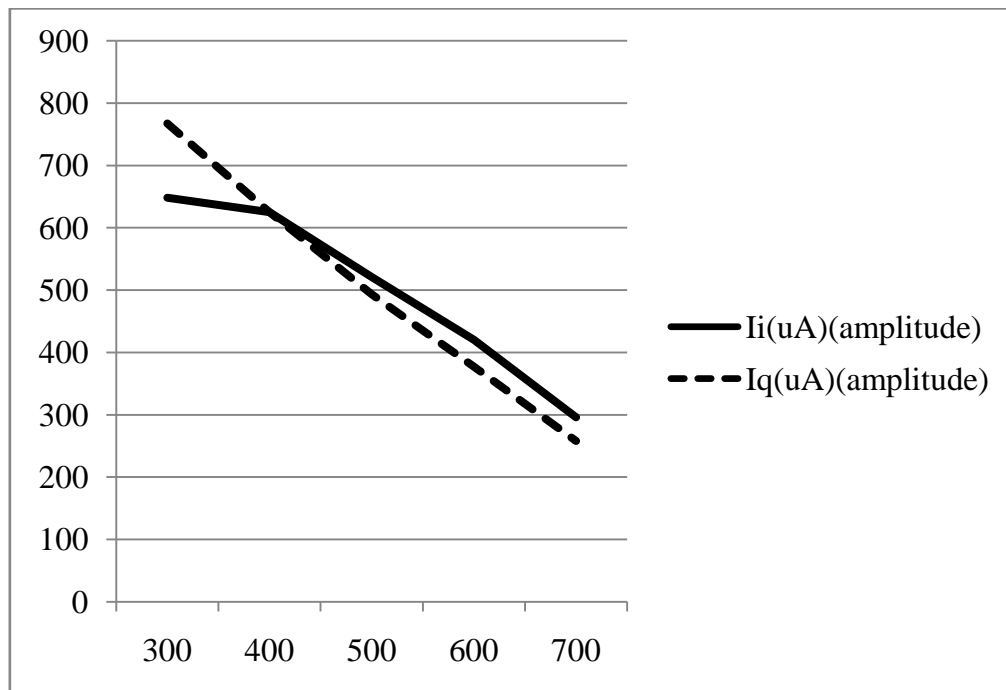


Fig. 13: the variation of current amplitudes versus change in resistance R_1

For verification of linearity performance, the THD (Total Harmonic Distortion) was calculated with MATLAB code. Figure 14 shows the obtained THD for voltage node V_i in various size of resistor R_1 . As shown in this figure, the linearity increases with increasing resistance, so it can be seen that the larger resistance decrease the frequency oscillation but increase the linearity and delay time and it can be trade-offs in oscillator design.

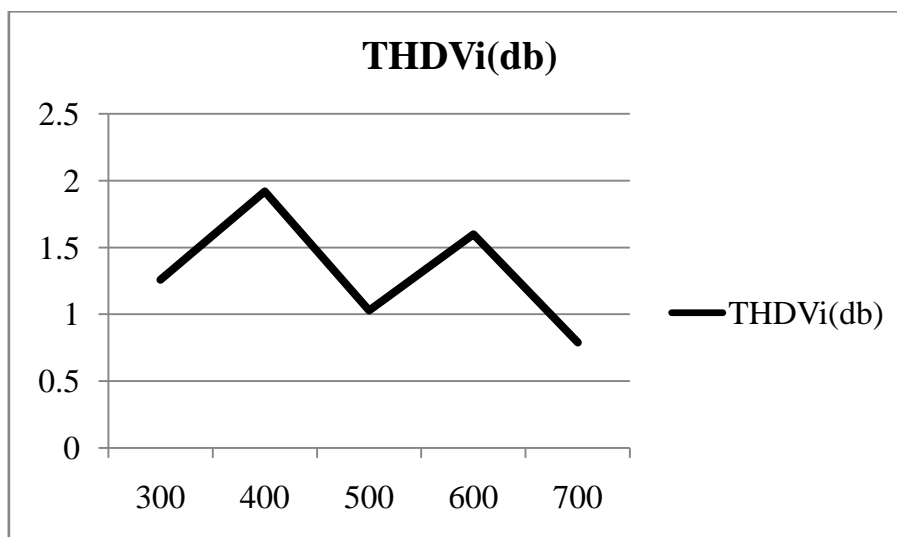


Fig. 14: the variation of THD versus change in resistance R_1

Conclusion:

In this paper, a class AB second generation current conveyor with CMOS transistors was designed and simulated. The proposed CCII have rail to rail linearity range in voltage and current transfer functions in comparison to other same works. The wide range bandwidth and low-voltage and low-power specifications were optimized. Furthermore, the proposed CCII has very low resistance at terminal x and it is capable to convert to other types by little changes in structure.

In the continuation of paper a multi-mode quadrature oscillator was designed and simulated. The especial features of the proposed circuit are low complexity, low voltage, low power, good linearity and high oscillation frequency. The circuit can be used in multi-mode analog structure because it able to construct a quadrature voltage or current outputs. The presented circuit can be implemented by the parallel switch resistance that it cause to make various frequency oscillations about one hundred MHz.

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